AFS

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	29

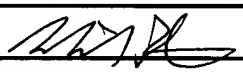
Application Number	09/820,079
Filing Date	March 28, 2001
First Named Inventor	Kloster, et al.
Art Unit	2811
Examiner Name	Magee, Thomas J.
Attorney Docket Number	P11026

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [✓] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please Identify below):

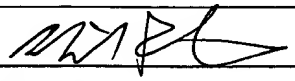
Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Intel Corporation		
Signature			
Printed name	Michael D. Plimier		
Date	December 1, 2005	Reg. No.	43,004

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Michael D. Plimier	Date	December 1, 2005

PTO/SB/17 (12-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/820,079
Filing Date	March 28, 2001
First Named Inventor	Kloster, et al.
Examiner Name	Magee, Thomas J.
Art Unit	2811
Attorney Docket No.	P11026

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0221 Deposit Account Name: Intel Corporation

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	0
Design	200	100	100	50	130	65	0
Plant	200	100	300	150	160	80	0
Reissue	300	150	500	250	600	300	0
Provisional	200	100	0	0	0	0	0

2. EXCESS CLAIM FEES

Fee Description	**Fee ($)**	**Small Entity Fee ($)**
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		**Extra Claims**	**Fee ($)**	**Fee Paid ($)**
_____	- 20 or HP =	_____	x _____ =	0

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**	**Fee ($)**	**Fee Paid ($)**
_____	- 3 or HP =	_____	x _____ =	0

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	**Fee Paid ($)**
_____	0

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**	**Number of each additional 50 or fraction thereof**	**Fee ($)**	**Fee Paid ($)**
_____	- 100 =	_____	/ 50 = _____ (round **up** to a whole number) x	_____ =	0

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	0
Other (e.g., late filing surcharge): Appeal Brief Under 37 C.F.R. section 41.37	500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 43,004	Telephone 408-765-7857
Name (Print/Type)	Michael D. Plimier		Date December 1, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Kloster, et al.

Serial No.: 09/820,079

Filed: March 28, 2001

For: **STRUCTURE IN A MICROELECTRONIC DEVICE INCLUDING A BI-LAYER FOR A DIFFUSION BARRIER AND AN ETCH STOP LAYER**

Art Unit: 2811

Examiner: Magee, Thomas J.

Attorney Docket: P11026

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

TABLE OF CONTENTS

(i) *Real party in interest.*

The real party in interest is the assignee, Intel Corporation.

(ii) *Related appeals and interferences.*

There are no known related appeals and / or interferences.

(iii) ***Status of claims.***

Claim 1 (Rejected)

Claim 2 (Canceled)

Claims 3-10 (Rejected)

Claim 11 (Canceled)

Claims 12-14 (Rejected)

Claim 15 (Canceled)

Claims 16-20 (Rejected)

Claims 21-27 (Canceled)

Claims 28-34 (Rejected)

Claims 35-38 (Canceled)

Claims 1, 3-10, 12-14, 16-20, and 28-34 are rejected and are the subject of this Appeal Brief.

(iv) ***Status of amendments.***

All filed amendments have been entered. The attached claims appendix reflects the current status of amendments as of the date of this appeal.

(v) *Summary of claimed subject matter.*

This patent application relates to a substrate (12, Figure 1) with a diffusion barrier layer (16, Figure 1) on the substrate, an etch stop layer (18, Figure 1) on the diffusion barrier layer, and an interlayer dielectric layer (ILD) (20, Figure 1) on the etch stop layer. Separate etch stop and diffusion barrier layers may provide an adequate etch stop and an adequate diffusion barrier while avoiding a high overall dielectric constant (low k-value) of the combined layers (Specification, page 6, lines 16-19), which may allow the structure to have a reduced resistance-capacitance delay of electrical signals going through interconnect pathways in the structure (Specification, page 5, lines 2-6).

Claim 1 recites a device with a structure, the structure including such layers. Claim 1 recites that the structure includes a diffusion barrier layer (16, Figure 1) that is above and on a substrate (12, Figure 1). The diffusion barrier layer has a thickness between about one atomic monolayer (Specification, page 14, line 1) and about 1000 angstroms (Specification, page 14, lines 3-4). The structure also includes an etch stop layer (18, Figure 1) above and on the diffusion barrier layer. The structure also includes an ILD layer (20, Figure 1) above and on the etch stop layer. The structure has an effective dielectric constant less than about 3 (Specification, page 14, lines 11-13).

Claim 9 recites a structure comprising such layers. The structure includes a substrate (12, Figure 1) with an upper surface and an electrically conductive trace (14, Figure 1) in the substrate. The structure also includes a diffusion barrier layer (16, Figure 1) that is above and on the substrate and the trace. The diffusion barrier layer has a thickness between about one atomic monolayer (Specification, page 14, line 1) and about 1000 angstroms (Specification, page 14, lines 3-4). The structure also includes an etch

stop layer (18, Figure 1) above and on the diffusion barrier layer. The diffusion barrier layer and the etch stop layer are mutually exclusively selected from either an organic composition or an inorganic composition (Specification, page 7, lines 7-9). The structure also includes an ILD layer (20, Figure 1) above and on the etch stop layer.

Claim 16 recites an article of manufacture comprising such layers. Claim 16 recite a semiconductor substrate (12, Figure 1). There is a first dielectric layer (16, Figure 1) is an inorganic composition (Specification, page 7, lines 1-2) that acts as a diffusion barrier on the substrate. The first dielectric layer has a thickness between about one atomic monolayer (Specification, page 14, line 1) and about 1000 angstroms (Specification, page 14, lines 3-4). There is an etch stop layer (18, Figure 1) that is an organic composition (Specification, page 7, lines 1-2) above and on the first dielectric layer. There is an ILD layer (20, Figure 1) disposed on the etch stop layer. There is a conductive damascene article (22, Figure 1) in contact with the substrate, the first dielectric layer, the etch stop layer, and the ILD layer.

(vi) ***Grounds of rejection to be reviewed on appeal.***

Independent claim 1:

I. Is claim 1 unpatentable over Chen (U.S. Patent Number 6,211,061) in view of Fink et al. ("Standard Handbook for Electrical Engr." McGraw-Hill, New York (1968))?

Claims dependent from claim 1:

II. Are claims 3 and 4 unpatentable over Chen in view of Fink and Wang (U.S. Patent Number 6,291,887)?

III. Are claims 5-7, and 29-33 unpatentable over Chen in view of Fink?

IV. Is claim 8 unpatentable over Chen in view of Fink and Dubin (U.S. Patent Number 6,249,055)?

V. Is claim 28 unpatentable over Chen in view of Fink and Uglow (U.S. Patent Number 6,251,770)?

VI. Is claim 34 unpatentable over Chen in view of Uglow?

Independent claim 9:

VII. Is claim 9 anticipated by Uglow?

Claims dependent from claim 9:

VIII. Is claim 10 anticipated by Uglow?

IX. Are claims 12-14 unpatentable over Uglow in view of Fink?

Independent claim 16:

X. Is claim 16 anticipated by Chen?

Claims dependent from claim 16:

XI. Are claims 17-18 anticipated by Chen?

XII. Is claim 19 unpatentable over Chen in view of Wolf ("Silicon Processing for the VLSI Era, Vol. 4 – Deep Submicron Process Technology," Lattice Press, Sunset Beach, CA (2002))?

XIII. Is claim 20 unpatentable over Chen in view of Bains ("Nanostructured Dielectrics Good Candidates for Next Generation Computer Chips," OE Reports, No. 194, (February, 2000))?

(vii) *Argument.*

I. The rejection of independent claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Fink is in error and should be reversed

Because the cited references fail to disclose or suggest each limitation of claim 1, the rejection is in error and should be overturned.

Chen and Fink fail to disclose or suggest a diffusion barrier layer on a substrate, an etch stop layer on the diffusion barrier layer, and an ILD layer on the etch stop layer as recited in claim 1. The Examiner has mischaracterized the dielectric layer (30) of Chen as an etch stop layer.[1] An etch stop layer is not merely defined by its composition, but rather its ability to stop an etch of another layer by virtue of its etch selectivity to the other layer (Detailed Description of the present invention page 7, lines 12-13, page 10, lines 21-22). Because a selected etch process will etch the etch stop layer at a **lesser** rate than the layer above it, the etch stop layer is used to stop an etch process used to etch a layer above the etch stop layer from affecting the layer below the etch stop layer.

The dielectric layer (30) in Chen is not an etch stop layer. In contrast, it is the opposite of an etch stop layer: it is etched at a **greater** rate than the layer above it (the hard mask layer (34)). Chen uses a hard mask layer (34) when patterning dielectric layer (30) (Chen, col. 6, lines 17-19; Fig. 4). Such hard mask layer-assisted patterning methods use the hard mask layer to protect the underlying patterned layer from the etchant, and the hard mask layer material is chosen to be etched at a **lower** rate than the layer below (thus, the layer below is etched at a greater rate than the hard mask layer). Thus, because the

[1] Office Action mailed July 8, 2005, page 2, first paragraph of section 4.

hard mask layer (34) above the dielectric layer (30) arrangement of Chen is the opposite of the ILD layer above an etch stop layer of claim 1, Chen fails to disclose or suggest an ILD layer above an etch stop layer as recited in claim 1. The rejection is in error and should be overturned.

II. The rejection of claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Fink and Wang is in error and should be reversed

The rejection of claims 3 and 4 should be overturned because there is no suggestion or motivation to combine the cited references to result in the structures recited in claim 3 and 4. A proper prima facie rejection under 35 U.S.C. 103(a) requires a suggestion or motivation within the cited prior art or within the knowledge generally available to one of ordinary skill in the art to combine references or modify a reference (MPEP 706.02(j), 2143; *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). The Examiner has failed to provide such a motivation found within the prior art.

Further, the motivation provided by the Examiner, "to obtain a dielectric layer stack with low 'effective' dielectric constant" would not result in one of skill in the art combining the references as suggested by the Examiner.[2] The Examiner had already stated that Chen when combined with Fink, even without the teaching of Wang, provides a low dielectric constant.[3] Thus, there would be no reason for one of skill in the art to further combine Wang to achieve a low dielectric constant, as that dielectric constant would have already been achieved. Because there is no motivation to combine Chen, Wang and Fink as suggested by the Examiner, the rejection should be overturned.

[2] Office Action mailed July 8, 2005, page 5, second paragraph of section 12.
[3] Office Action mailed July 8, 2005, first paragraph of page 3.

III. The rejection of claims 5-7, and 29-33 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Fink is in error and should be reversed

Claims 5-7, 29, and 31-32 depend from claim 1. Rejections of these claims are in error and should be overturned for the reasons provided above.

In addition, Chen fails to disclose or suggest a structure with an ILD layer thickness at least five times as that of a second layer, and an effective dielectric constant of less than about 3, as recited in claims 30 and 33.

The rejection of claims 30 and 33 should be overturned because there is no suggestion or motivation to combine the cited references to result in a structure with an ILD layer thickness at least five times as thick as the thickness of the etch stop layer, as recited in claims 30 and 33. The Examiner characterized layer (30) of Chen as an etch stop layer and layer (34) of Chen as an ILD layer.[4] The Examiner's suggested motivation, "to reduce parasitic capacitance,"[5] would not lead one of skill in the art to create a structure where layer (34) of Chen is at least five times the thickness of layer (30) of Chen.

Rather, such a motivation would cause one of skill in the art to do the opposite: minimize the thickness of layer (34) relative to layer (30). Layer (34) of Chen is a hard mask layer that is composed of silicon dioxide or silicon oxynitride (Chen, col. 6, lines 13-17), neither of which are low-k, and layer (30) of Chen is a low-k dielectric layer (Chen, col. 6, lines 8-9). Thus, if one of skill in the art were motivated to reduce the parasitic capacitance as suggested by the Examiner (and the Examiner failed to cite any prior art reference as providing such a motivation), that person would be motivated to

[4] Office Action mailed July 8, 2005, page 2, first paragraph of section 4.

minimize the thickness of relatively high-k layer (34) relative to the thickness of low-k layer (30), not the other way around.

The obvious falsehood of one of skill in the art providing more high-k material and less low-k material in order to reduce parasitic capacitance (when in fact this would increase parasitic capacitance) highlights the fact that the Examiner has mischaracterized the layers of Chen in attempting to reject claim 1.

Further, as stated by the Examiner in the rejection of claim 1, layer (34) of Chen has a dielectric constant of 3.9, layer (30) of Chen has a dielectric constant of less than 3.0, and layer (24) of Chen has a dielectric constant of over 7.[6] If layer (34) of Chen were at least five times as thick as layer (30), the dielectric constant of layer (30) would have to be under 1.5 for the effective dielectric constant of the structure to be under about 3. Chen fails to disclose or suggest a layer (30) with a dielectric constant of under 1.5. Thus, even if one of skill in the art, armed with the knowledge of Chen, would be motivated to make the ILD layer at least five times as thick as the etch stop layer (and Applicants dispute this), the resulting structure would have an effective dielectric constant above 3.

IV. The rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Fink and Dubin is in error and should be reversed

Claim 8 depends from claim 1. As shown above, Chen and Fink fail to disclose each limitation of claim 1. Dubin fails to rectify this deficiency. The rejection should be overturned.

---

[5] Office Action mailed July 8, 2005, page 4, sections 8 and 11.
[6] Office Action mailed July 8, 2005, page 2, first paragraph of section 4.

V. The rejection of claim 28 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Fink and Uglow is in error and should be reversed

Claim 28 depends from claim 1. As shown above, Chen and Fink fail to disclose each limitation of claim 1. Uglow fails to rectify this deficiency. The rejection should be overturned.

VI. The rejection of claim 34 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view Uglow is in error and should be reversed

Claim 34 depends from claim 1. As shown above, Chen fails to disclose each limitation of claim 1. Uglow fails to rectify this deficiency. The rejection should be overturned.

Further, claim 34, like claims 30 and 33, recites a structure with an ILD layer thickness at least five times as that of an etch stop layer, and an effective dielectric constant of less than about 3. As shown above with respect to claims 30 and 33, Chen fails to disclose or suggest this. Uglow similarly fails to disclose or suggest such a structure.

VII. The rejection of claim 9 under 35 U.S.C. § 102[7] as being anticipated by Uglow is in error and should be reversed

Uglow fails to disclose both a diffusion barrier layer on a substrate and an etch stop layer on the diffusion barrier layer, as is recited in claim 9. As stated at page 3, lines 18-19 of the Specification, prior art devices used a single layer as an etch stop and a diffusion barrier (Specification, page 3, lines 18-19). Such devices with one layer being

[7] Note that the Office Action mailed July 8, 2005, at page 10, states that claims 9 and 10 are rejected under 35 U.S.C. 103. However, since the rejections are set out under the heading of claim rejections under 35 U.S.C. 102, and the term "anticipated" is used, Applicants believe the use of 35. U.S.C. 103 in the rejection was a typo.

both an etch stop and a diffusion barrier, negatively impact the overall dielectric constant between metal lines (Specification, page 3, line 20 through page 4, line 2). Devices with separate diffusion barrier and etch stop layers may improve the dielectric constant (Specification, page 5, lines 2-6). Claim 9 recites such a device.

Uglow, in contrast, fails to disclose both a diffusion barrier layer on a substrate and a separate etch stop layer on the diffusion barrier layer. Uglow explicitly states that barrier layer 102 is both a barrier layer and an etch stop layer (Uglow, col. 4, lines 40-41), exactly like the prior art identified by the Applicants. The Examiner incorrectly characterizes the via dielectric layer 104 of Uglow as an etch stop layer. Not only does this characterization contradict the teaching of Uglow, but because barrier layer 102 is an etch stop, it would make no sense for via dielectric layer 104, directly above barrier layer 102, to also be an etch stop layer. Thus, Uglow fails to disclose both a diffusion barrier layer and a separate etch stop layer as is recited in claim 9. The rejection should be overturned.

Further, assuming, *arguendo*, the Examiner's characterization of the via dielectric layer 104 of Uglow as an etch stop layer[8] is correct, Uglow fails to disclose a diffusion barrier layer and an etch stop layer "mutually **exclusively** selected" (emphasis added) from either an organic compound or an inorganic compound, as is recited in claim 9. With such mutually exclusively selected materials, if the diffusion barrier layer is organic, the etch stop layer is inorganic, for example, or vice versa (Specification, page 7, lines 7-9). In making the rejection, the Examiner ignores the word "exclusively" in the claim 9. In fact, the Examiner, in making the rejection, states that Uglow teaches the diffusion

barrier and etch stop layer are "mutually selected" from an inorganic composition (note the absence of the word "exclusively").[9] The Examiner is correct. Uglow teaches a diffusion barrier and etch stop layer mutually selected from an inorganic composition. Rather than one of the diffusion barrier layer and etch stop layer being organic and the other inorganic as recited in the claim, Uglow teaches that both are inorganic. However, as the claim recites the opposite, that the diffusion barrier layer and the etch stop layer are "mutually **exclusively** selected" from either an organic compound or an inorganic compound, such a teaching does not support a rejection of claim 9. The rejection should be overturned.

VIII. The rejection of claim 10 under 35 U.S.C. § 102 as being anticipated by Uglow is in error and should be reversed

Claim 10 depends from claim 9. Uglow thus fails to anticipate claim 10 for the same reasons given with respect to claim 9, above.

IX. The rejection of claims 12-14 under 35 U.S.C. § 103(a) as being unpatentable over Uglow in view of Fink is in error and should be reversed

Claims 12-14 depend from claim 9. As shown above, Uglow fails to disclose each limitation of claim 9. Fink fails to rectify this deficiency. The rejection should be overturned.

X. The rejection of independent claim 16 under 35 U.S.C. § 102 as being anticipated by Chen is in error and should be reversed

As stated above with respect to claim 1, Chen fails to disclose a diffusion barrier layer on a substrate, an etch stop layer on the diffusion barrier layer, and an ILD layer on

[8] Office Action mailed July 8, 2005, page 10, first paragraph of section 24.

the etch stop layer, as is recited in claim 16. The rejection is in error and should be overturned.

XI. The rejection of claims 17 and 18 under 35 U.S.C. § 102 as being anticipated by Chen is in error and should be reversed

Claims 17 and 18 depend from claim 16. Chen thus fails to disclose each limitation of claims 17 and 18 for the reasons provided above.

XII. The rejection of claim 19 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Wolf is in error and should be reversed

Claim 19 depends from claim 16. As shown above, Chen fails to disclose each limitation of claim 16. Wolf fails to rectify this deficiency. The rejection should be overturned.

XIII. The rejection of claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Bains is in error and should be reversed

Claim 20 depends from claim 16. As shown above, Chen fails to disclose each limitation of claim 16. Bains fails to rectify this deficiency. The rejection should be overturned.

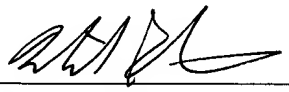
[9] Office Action mailed July 8, 2005, page 10, first paragraph of section 24.

CONCLUSION

For the foregoing reasons, applicant respectfully requests the Board to vacate the examiner's rejections of claims 1, 3-10, 12-14, 16-20, and 28-34, to remand this application to the Examiner, and to direct the Examiner to pass this case to issuance.

Respectfully submitted,

Date: December 1, 2005



Michael Plimier
Reg. No: 43,004
ATTORNEY FOR APPLICANTS

Intel Corporation
Mail Stop SC4-202
2200 Mission College Blvd.
Santa Clara, CA 95052-8119
(408) 765-7857

(viii) ***Claims appendix.***

1. In a microelectronic device, a structure on a substrate comprising:

a diffusion barrier layer disposed above and on the substrate, the diffusion barrier layer having a first thickness and a first dielectric constant, wherein the first thickness comprises a range from about one atomic monolayer to about 1000 angstroms;

an etch stop layer above and on the diffusion barrier layer, the etch stop layer having a second thickness, and a second dielectric constant; and

an interlayer dielectric (ILD) layer disposed above and on the etch stop layer, wherein the structure has an effective dielectric constant in a range less than about 3.

3. The structure according to claim 1, wherein the diffusion barrier layer comprises an organic composition and wherein the etch stop layer comprises an inorganic composition.

4. The structure according to claim 1, wherein the diffusion barrier layer is selected from arylene, parylene, and arylene ether polymers, and fluorinated polyimides.

5. The structure according to claim 1, wherein the diffusion barrier layer comprises an inorganic composition and wherein the etch stop layer comprises an organic composition.

6. The structure according to claim 1, wherein the etch stop layer comprises an organic composition and wherein the diffusion barrier layer is selected from silicon nitride, silicon oxide, silicon oxynitride, aluminum oxide, aluminum nitride, aluminum oxynitride, beryllium oxide, beryllium nitride, beryllium oxynitride, boron oxide, boron nitride, boron oxynitride, cerium oxide, cerium nitride, cerium oxynitride, yttrium oxide, yttrium nitride, yttrium oxynitride, carbon-doped oxide, carbon nitride, carbon oxynitride, a ceramic dielectric, and combinations thereof.

7. The structure according to claim 1, further comprising:

an electrically conductive trace disposed in the substrate; and

a contact disposed in a recess that extends through the ILD layer, the etch stop layer, and the diffusion barrier layer, and wherein the contact makes an electrical connection to the trace.

8. The structure according to claim 1, further comprising:

an electrically conductive trace disposed in the substrate; and

a contact disposed in a recess that extends through the ILD layer, the etch stop layer, and the diffusion barrier layer, and wherein the contact makes an electrical connection to the trace, wherein the contact is a single-damascene contact article.

9. In a microelectronic device, a structure comprising:

a substrate having an upper surface;

an electrically conductive trace in the substrate;

a diffusion barrier layer disposed above and on the substrate and the trace, wherein the diffusion barrier layer comprises a thickness in a range from about one atomic monolayer to about 1000 angstroms;

an etch stop layer above and on the diffusion barrier layer; and

an ILD layer disposed above and on the etch stop layer, wherein the diffusion barrier layer and the etch stop layer are mutually exclusively selected from either an organic composition or an inorganic composition.

10. The structure according to claim 9, wherein the trace surface is coplanar to the upper surface.

12. The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient less than about 3.

13. The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient of about 2.8.

14. The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient in a range from about 2.6 to about 2.8.

16. An article of manufacture comprising:

a semiconductor substrate;

a first dielectric layer disposed on the semiconductor substrate, wherein the first dielectric layer comprises a thickness in a range from about one atomic monolayer to about 1000 angstroms;

an etch stop layer disposed above and on the first dielectric layer;

an interlayer dielectric (ILD) disposed on the etch stop layer; and

a conductive damascene article, wherein the conductive damascene article is in contact with the substrate, the first dielectric layer, the etch stop layer, and the ILD layer;

and wherein the first dielectric layer is an inorganic composition and comprises a material selected to be a diffusion barrier to prevent diffusion of material of the conductive damascene article into the substrate, and wherein the etch stop layer is an organic composition.

17. The article of claim 16, wherein the first dielectric layer is selected from silicon nitride, silicon oxide, silicon oxynitride, aluminum oxide, aluminum nitride, aluminum oxynitride, beryllium oxide, beryllium nitride, beryllium oxynitride, boron oxide, boron nitride, boron oxynitride, cerium oxide, cerium nitride, cerium oxynitride, yttrium oxide, yttrium nitride, yttrium oxynitride, carbon-doped oxide, carbon nitride, carbon oxynitride, a ceramic dielectric, and combinations thereof.

18. The article of claim 16, wherein the etch stop layer is selected from arylene, parylene, and arylene ether polymers, and fluorinated polyimides.

19. The article of claim 16, wherein the etch stop layer has a dielectric constant in a range of less than about 2.8.

20. The article of claim 16, wherein the etch stop layer has a dielectric constant in a range of about 2.

28. The structure according to claim 1, further comprising:

an electrically conductive trace disposed in the substrate;

a first recess in the ILD layer with a first width and extending from a bottom surface of the ILD layer up to a position partway through the ILD layer;

a second recess in the ILD layer with a second width wider than the first width and extending from the top of the first recess to the top of the ILD layer; and

a contact disposed in the first and second recesses, wherein the contact makes an electrical connection to the trace.

29. The structure according to claim 1, wherein:

the ILD layer has a third thickness; and

the third thickness is greater than the second thickness.

30. The structure according to claim 1, wherein:

the ILD layer has a third thickness; and

the third thickness is at least about 5 times as thick as the second thickness.

31. The structure according to claim 1, wherein the second thickness is greater than the first thickness.

32. The structure according to claim 1, wherein the second thickness is at least about 10 times as thick as the first thickness.

33. The structure according to claim 1, wherein:

the ILD layer has a third thickness;

the third thickness is at least about 5 times as thick as the second thickness; and

the second thickness is at least about 10 times as thick as the first thickness.

34. The structure according to claim 1, wherein:

the diffusion barrier layer comprises silicon nitride;

the etch stop layer comprises an organic polymer;

the ILD layer comprises a carbon doped oxide and has a third thickness;

the third thickness is at least about 5 times as thick as the second thickness; and

the second thickness is at least about 10 times as thick as the first thickness.

FIRST CLASS CERTIFICATE OF MAILING

(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 1, 2005.

Michael D. Plimier
Name of Person Mailing Correspondence

Signature

December 1, 2005
Date